

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltages are absolute voltages referenced to COM. Thermal resistance and power dissipation are measured under board mounted and still air conditions.

| Parameters | Symbols | Min. | Max. | Units | Remarks |
|---------------------------|---------------------|------|------|-------|--------------------------------|
| V _{CC} voltage | V _{CC} | -0.3 | 22 | V | Not internally clamped |
| Freq. voltage | V _{FREQ.} | -0.3 | 10.5 | V | |
| I _{SNS} voltage | V _{ISNS} | -10 | 3 | V | |
| V _{FB} voltage | V _{FB} | -0.3 | 10.5 | V | |
| COMP voltage | V _{COMP} | -0.3 | 10 | V | |
| Gate voltage | V _{GATE} | -0.3 | 18 | V | |
| Continuous gate current | I _{GATE} | -5 | 5 | mA | |
| Max peak gate current | I _{GATEPK} | -1.5 | 1.5 | A | |
| Junction temperature | T _J | -40 | 150 | °C | |
| Storage temperature | T _S | -55 | 150 | °C | |
| Thermal resistance | R _{θJA} | — | 128 | °C/W | SOIC-8 |
| | | — | 84 | °C/W | PDIP-8 |
| Package power dissipation | P _D | — | 675 | mW | SOIC-8 T _{AMB} = 25°C |
| | | — | 1000 | mW | PDIP-8 T _{AMB} = 25°C |
| ESD protection | V _{ESD} | — | 2 | kV | Human body model* |

Recommended Operating Conditions

Recommended operating conditions for reliable operation with margin

| Parameters | Symbols | Min. | Typ. | Max. | Units | Remarks |
|----------------------|-----------------|------|------|------|-------|------------|
| Supply voltage | V _{CC} | 15 | 18 | 20 | V | |
| Junction temperature | T _J | -25 | — | 125 | °C | |
| Ambient temperature | T _A | 0 | — | 70 | °C | IR1150(S) |
| Ambient temperature | T _A | -25 | — | 85 | °C | IR1150I(S) |
| Switching frequency | F _{SW} | 50 | — | 200 | kHz | |

Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25 °C to 125°C. Typical values represent the median values, which are related to 25°C. **If not otherwise stated, a supply voltage of V_{CC} = 15V is assumed for test condition**

Supply Section

| Parameters | Symbols | Min. | Typ. | Max. | Units | Remarks |
|-------------------------------------------------------------|----------------------|------|------|------|-------|---------|
| V _{CC} turn-on threshold | V _{CC ON} | 12.2 | 12.7 | 13.2 | V | |
| V _{CC} turn-off threshold (under voltage lock out) | V _{CC UVLO} | 10.2 | 10.7 | 11.2 | V | |

*Per EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5KΩ series resistor)

Electrical Characteristics cont.

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_j from -25°C to 125°C . Typical values represent the median values, which are related to 25°C . If not otherwise stated, a supply voltage of $V_{CC} = 15\text{V}$ is assumed for test condition.

| Parameters | Symbols | Min. | Typ. | Max. | Units | Remarks |
|------------------------------|----------------|------|------|------|---------------|-------------------------------------------------------------|
| V_{CC} turn-off hysteresis | $V_{CC\ HYST}$ | 1.8 | — | 2.2 | V | |
| Operating current | I_{CC} | — | 18 | 22 | mA | $C_{LOAD}=1\text{nF } f_{SW}=200\text{kHz}$ |
| | | — | 36 | 40 | mA | $C_{LOAD}=10\text{nF } f_{SW}=200\text{kHz}$ |
| | | — | 8 | 10 | mA | Standby mode - inactive gate Internal oscillator running |
| Startup current | $I_{CCSTART}$ | — | — | 175 | μA | $V_{CC}=V_{CC\ ON} -0.1\text{V}$ |
| Sleep current | I_{SLEEP} | — | 125 | 200 | μA | $V_{OVP}<0.5\text{V (typ)}, V_{CC} = 15\text{V}$ |

Oscillator Section

| Parameters | Symbols | Min. | Typ. | Max. | Units | Remarks |
|-----------------------|---------------|------|------|------|-------|----------------------------------------------------------|
| Switching frequency | f_{SW} | 50 | — | 200 | kHz | $R_{SET} = 165\text{k}\Omega - 37\text{k}\Omega$ approx. |
| Initial accuracy | $f_{SW\ ACC}$ | — | — | 5 | % | $T_A = 25^{\circ}\text{C}$ |
| Voltage stability | V_{STAB} | — | 0.2 | 3 | % | $13\text{V} < V_{CC} < 20\text{V}$ |
| Temperature stability | T_{STAB} | — | 2 | — | % | $-25^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ |
| Total variation | f_{VT} | — | 10 | — | % | Line & temperature |
| Long term stability | $F_{STABL T}$ | — | 0.1 | 0.5 | % | $T_{AMB} = 125^{\circ}\text{C}, 1000\text{Hrs}$ |
| Maximum duty cycle | D_{MAX} | 93 | — | 98 | % | $f_{SW}=200\text{kHz}$ |
| Minimum duty cycle | D_{MIN} | — | — | 0 | % | |
| Minimum off time | T_{offmin} | 200 | 300 | 400 | ns | $f_{SW}=50\text{kHz to } 200\text{kHz}$ |

Protection Section

| Parameters | Symbols | Min. | Typ. | Max. | Units | Remarks |
|------------------------------------------------------------------------------|------------|-------|-------|-------|-------------|----------------------|
| Open loop protection (OLP) Vfb threshold | V_{OLP} | 17 | 19 | 21 | % V_{REF} | |
| Output under voltage protection (OUV) | V_{OUV} | 49 | 51 | 53 | % V_{REF} | Brown out protection |
| Output over voltage protection (OVP) | V_{OVP} | 104 | 105.5 | 107 | % V_{REF} | |
| OVP hysteresis | — | 350 | 450 | 550 | mV | |
| Peak current limit protection (I_{PKLMT}) I_{SNS} voltage threshold | V_{ISNS} | -1.11 | -1.04 | -0.96 | V | |

Internal Voltage Reference Section

| Parameters | Symbols | Min. | Typ. | Max. | Units | Remarks |
|-------------------|------------------|------|------|------|-------|---------------------------------------------------------|
| Reference voltage | V_{REF} | 6.9 | 7.0 | 7.1 | V | $T_A = 25^\circ\text{C}$ |
| Line regulation | R_{REG} | — | 12 | 25 | mV | $13.5\text{V} < V_{CC} < 20\text{V}$ |
| Temp stability | T_{STAB} | — | 0.4 | — | % | $-25^\circ\text{C} \leq T_{AMB} \leq 125^\circ\text{C}$ |
| Total variation | ΔV_{TOT} | 6.8 | — | 7.1 | V | Over V_{CC} and T_j ranges |

Voltage Error Amplifier Section

| Parameters | Symbols | Min. | Typ. | Max. | Units | Remarks |
|---------------------------------------|-------------------|------|------|------|------------------------------|----------------------------------------------------------------------------------------------------------------------|
| Transconductance | g_m | 30 | 40 | 55 | μS | $-25^\circ\text{C} \leq T_{AMB} \leq 125^\circ\text{C}$ |
| Source/sink current | I_{OEA} | 30 | 40 | 65 | μA | $T_{AMB} = 25^\circ\text{C}$ |
| | | 20 | 45 | 90 | μA | $-25^\circ\text{C} \leq T_{AMB} \leq 125^\circ\text{C}$ |
| Soft start delay time (calculated) | t_{ss} | — | 40 | — | ms | $R_{GAIN} = 1\text{k}\Omega$, $C_{ZERO} = 0.33\mu\text{F}$ $C_{POLE} = 0.01\mu\text{F}$, $f_{XO} = 28\text{Hz}$ |
| V_{COMP} voltage (fault) | $V_{COMP\ FLT}$ | — | 1.2 | 1.5 | V | @ 1mA (max) initial |
| | | | | 0.2 | V | @ 25 μA steady state |
| Effective V_{COMP} voltage | $V_{COMP\ EFF}$ | | 6.05 | | V | |
| Input bias current | I_{IB} | — | -0.2 | -0.5 | μA | $V_{FB} = 0\text{V}$, $-25^\circ\text{C} \leq T_{AMB} \leq 125^\circ\text{C}$ |
| Open loop bandwidth | BW | — | 1 | — | MHz | |
| Input offset voltage temp coefficient | TC_{IOV} | — | — | 10 | $\mu\text{V}/^\circ\text{C}$ | Note 1 |
| Common mode rejection ratio | CMRR | — | 100 | — | dB | |
| Output low voltage | V_{OL} | — | — | 0.5 | V | |
| Output high voltage | V_{OH} | 5.71 | 6.15 | 6.8 | V | |
| V_{COMP} start voltage | $V_{COMP\ START}$ | 300 | 500 | 700 | mV | |

Current Amplifier Section

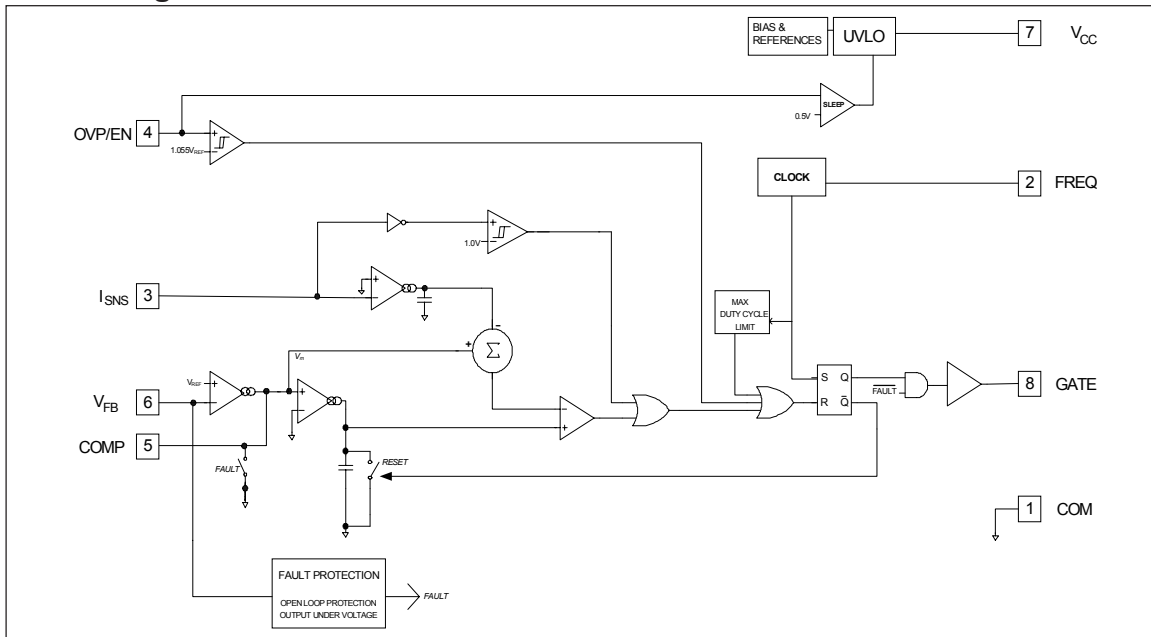
| Parameters | Symbols | Min. | Typ. | Max. | Units | Remarks |
|---------------------------------------|-------------|------|------|------|------------------------------|--------------------------------------------------------------------------------|
| DC gain | g_{DC} | — | 2.5 | — | V/V | |
| Corner frequency | f_C | 200 | — | 280 | kHz | Note 1 |
| Input offset voltage | V_{IO} | — | 1 | 4 | mV | Note 1 |
| I_{SNS} bias current | I_{IB} | — | 200 | 300 | μA | $V_{FB} = 0\text{V}$, $-25^\circ\text{C} \leq T_{AMB} \leq 125^\circ\text{C}$ |
| Input offset voltage temp coefficient | TC_{IOV} | — | — | 10 | $\mu\text{V}/^\circ\text{C}$ | Note 1 |
| Common mode rejection ratio | CMRR | — | 100 | — | dB | |
| Blanking time | T_{BLANK} | 230 | 350 | 450 | ns | $T_{AMB} = 25^\circ\text{C}$ |
| | | 150 | | 600 | ns | $-25^\circ\text{C} \leq T_{AMB} \leq 125^\circ\text{C}$ |

Gate Driver Section

| Parameters | Symbols | Min. | Typ. | Max. | Units | Remarks |
|----------------------|----------------------|------|------|------|-------|------------------------------------------------|
| Gate low voltage | V _{GLO} | — | 1.2 | 1.5 | V | I _{GATE} =200mA |
| Gate high voltage | V _{GTH} | — | 13 | 18 | V | V _{CC} =20V |
| Gate high voltage | V _{GTH} | 9.5 | — | — | V | V _{CC} =11.5V |
| Rise time | t _r | — | 20 | — | ns | C _{LOAD} = 1nF, V _{CC} =16V |
| | | — | 70 | — | ns | C _{LOAD} = 10nF, V _{CC} =16V |
| Fall time | t _f | — | 20 | — | ns | C _{LOAD} = 1nF, V _{CC} =16V |
| | | — | 70 | — | ns | C _{LOAD} = 10nF, V _{CC} =16V |
| Out peak current | I _{OPK} | 1.5 | — | — | A | C _{LOAD} = 10nF, V _{CC} =16V |
| Gate voltage @ fault | V _{G fault} | — | — | 1.8 | V | I _{GATE} =20mA |

Note 1: Guaranteed by design, but not tested in production.

Block Diagram



Lead Assignments & Definitions

| Lead Assignment | Pin# | Symbol | Description |
|--------------------------------------------------|------|------------------|-----------------------------------|
| <p style="text-align: center;">IR1150</p> | 1 | COM | Ground |
| | 2 | FREQ | Frequency Set |
| | 3 | I _{SNS} | Current Sense |
| | 4 | OVP/EN | Overvoltage Fault Detect / Enable |
| | 5 | COMP | Voltage Loop Compensation |
| | 6 | V _{FB} | Output Voltage Sense |
| | 7 | V _{CC} | IC Supply Voltage |
| | 8 | GATE | Gate Drive Output |

General Description

The μ PFC IR1150 is intended for boost converters for power factor correction operating at a fixed frequency in continuous conduction mode. The IC operates with two loops; an inner current loop and an outer voltage loop. The inner current loop is fast, reliable and does not require sensing of the input voltage in order to create a current reference.

This inner current loop sustains the sinusoidal profile of the average input current based on the dependency of the pulse width modulator duty cycle on the input line voltage in order to determine the analogous input line current. Thus, the current loop uses the embedded input voltage signal to control the average input current to follow the input voltage.

The IR1150 enables excellent THD performance. In light load conditions, a small distortion occurs at zero-crossing due to the finite boost inductance but this is negligible and well within EN61000-3-2 Class D specifications.

The outer voltage loop controls the DC bus voltage. This voltage is fed into the voltage error amplifier to control the slope of the integrator ramp and sets the amplitude of the average input current.

The two loops combine to control the amplitude, phase and shape of the input current, with respect to the input voltage, giving near-unity power factor.

The IC is designed for robust operation and provides protection from system level over current, over voltage, under voltage, and brownout conditions.

IC Supply

The UVLO circuit monitors the V_{CC} pin and maintains the gate drive signal inactive until the V_{CC} pin voltage reaches the UVLO turn on threshold, ($V_{CC\ ON}$). As soon as the V_{CC} voltage exceeds this threshold, provided that the V_{FB} pin voltage is greater than $20\%V_{REF}$, the gate drive will begin switching (under Soft Start) and increase the pulse width to its maximum value as demanded by the output voltage error amplifier. If the voltage on the V_{CC} pin falls below the UVLO turn off threshold, ($V_{CC\ UVLO}$), the IC turns off, gate drive is terminated, and the turn on threshold must again be exceeded in order to re-start the process and move into Soft Start mode.

Soft Start

Soft Start controls the rate of rise of the output voltage error amplifier in order to obtain a linear control of the increasing duty cycle as a function of time. The Soft Start time is controlled by voltage error amplifier compensation components selected, and is user programmable based on desired loop crossover frequency.

Frequency Select

The switching frequency of the IC is programmable by an external resistor at the $FREQ$ pin. The design incorporates min/max restrictions such that the minimum and maximum operating frequency fall within the range of 50-200kHz.

Gate Drive

The gate drive is a totem pole driver with 1.5A capability. If higher currents are required, additional external drivers can be used.

Detailed Pin Description

COM: Ground

This is the ground potential pin of the integrated control circuit. All internal devices are referenced to this point.

V_{FB}: Output Voltage Feedback

The output voltage of the boost converter is sensed via a resistive divider and fed into this pin, which is the inverting input of the output voltage error amplifier. The impedance of the divider string must be low enough so as to not introduce substantial error due to the input bias currents of the amplifier, yet high enough so as to minimize power dissipation. A typical value of external divider impedance is 1M Ω .

The error amplifier is a transconductance type which yields high output impedance, thus increasing the noise immunity of the error amplifier output. This also eliminates input divider string interaction with compensation feedback capacitors and reducing the loading of divider string due to a low impedance output of the amplifier.

COMP: Voltage Loop Compensation

External circuitry from this pin to ground compensates the system voltage loop and soft start time. This is the output of the voltage error amplifier. This pin will be discharged via internal resistance when a fault mode occurs.

GATE: Gate Drive Output

This is the gate drive output of the IC. Drive voltage is internally limited and provides $\pm 1.5A$ peak with matched rise and fall times.

FREQ: Frequency Set

This is the user programmable frequency pin. An external resistor from this pin to the COM pin programs the frequency. The operational switching frequency range for the device is 50kHz – 200kHz.

I_{SNS}: Current Sense input

This pin is the inverting Current Sense Input & Peak Current Limit. The voltage at this pin is the negative voltage drop, sensed across the system current sense resistor, representing the inductor current.

This voltage is fed into the Peak Current Limit protection comparator with threshold around -1V. This protection circuit incorporates a leading edge blanking circuit following the comparator to improve noise immunity of the protection process.

The current sense signal is also fed into the current sense amplifier. The signal is amplified, filtered of high frequency noise and then injected into a summing node where it is subtracted from the compensation voltage V_{COMP}.

The signal on this pin must be previously filtered with an RC cell to provide additional noise immunity. The input impedance of this pin is 5k Ω .

V_{CC}: Supply Voltage

This is the supply voltage pin of the IC and it is monitored by the under voltage lockout circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, without damage to the IC.

To prevent noise problems, a bypass ceramic capacitor connected to V_{CC} and COM should be placed as close as possible to the IR1150.

This pin is not internally clamped, therefore damage will occur if the maximum voltage is exceeded.

OVP/EN: Over Voltage Protection / Enable

This pin is the input to the over voltage protection comparator the threshold of which is internally programmed to 105.5% of V_{REF}.

A resistive divider feeds this pin from the output voltage to COM and inhibits the gate drive whenever the threshold is exceeded. Normal operation resumes when the voltage level on this pin decreases to below the pin threshold.

This pin is also used to activate “sleep” mode by pulling the voltage level below 0.62V (typ).

Operating States

UVLO Mode

The IC remains in the UVLO condition until the voltage on the V_{CC} pin exceeds the V_{CC} turn on threshold voltage, $V_{CC\ ON}$.

During the time the IC remains in the UVLO state, the gate drive circuit is inactive and the IC draws a quiescent current of $I_{CC\ START}$. The UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of $V_{CC} < V_{CC\ UVLO}$ occurs.

Standby Mode

The IC is in this state if the supply voltage has exceeded $V_{CC\ ON}$ and the V_{FB} pin voltage is less than 20% of V_{REF} . The oscillator is running and all internal circuitry is biased in this state but the gate is inactive. This state is accessible from any other state of operation except OVP. The IC enters this state whenever the V_{FB} pin voltage has decreased to 50% of V_{REF} when operating in normal mode or during a peak current limit fault condition, or 20% V_{REF} when operating in soft start mode.

Soft Start Mode

This state is activated once the V_{CC} voltage has exceeded $V_{CC\ ON}$ and the V_{FB} pin voltage has exceeded 20% of V_{REF} .

The soft start time, which is defined as the time required for the duty cycle to linearly increase from zero to maximum, is dependent upon the values selected for compensation of the voltage loop pin COMP to pin COM. Throughout the soft start cycle, the output of the voltage error amplifier (pin COMP) charges through the compensation network. This forces a linear rise of the voltage at this node which in turn forces a linear increase in the gate drive duty cycle from 0. This controlled duty cycle reduces system component stress during start up conditions as the input current amplitude is increasing linearly.

Normal Mode

The IC enters normal operating mode once the soft start transition has been completed. At this point the gate drive is switching and the IC draws a maximum of I_{CC} from the supply voltage source. The device will initiate another soft start sequence in the event of a shutdown due to a fault, which activates the protection circuitry, or if the supply voltage drops below the UVLO turn off threshold of $V_{CC\ UVLO}$.

Fault Protection Mode

The fault mode will be activated when any of the protection circuits are activated. The IC protection circuits include Supply Voltage Under Voltage Lockout (UVLO), Output Over Voltage Protection (OVP), Open Loop Protection (OLP), Output Undervoltage Protection (OUV), and Peak Current Limit Protection ($I_{PK\ LIMIT}$).

Sleep Mode

The sleep mode is initiated by pulling the OVP pin below 0.62V (typ). In this mode the IC draws a very low quiescent supply current.

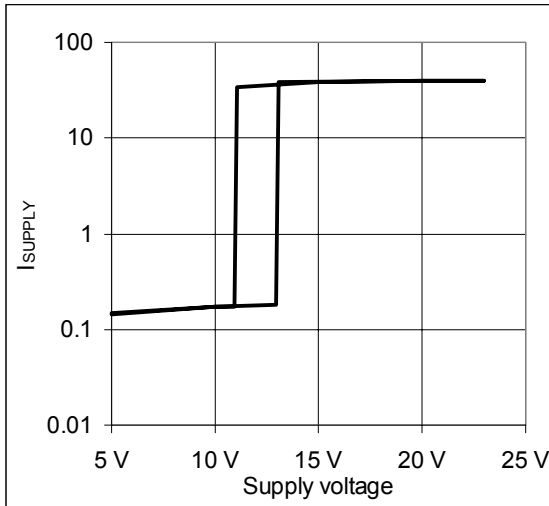


Fig.1 - Supply Current

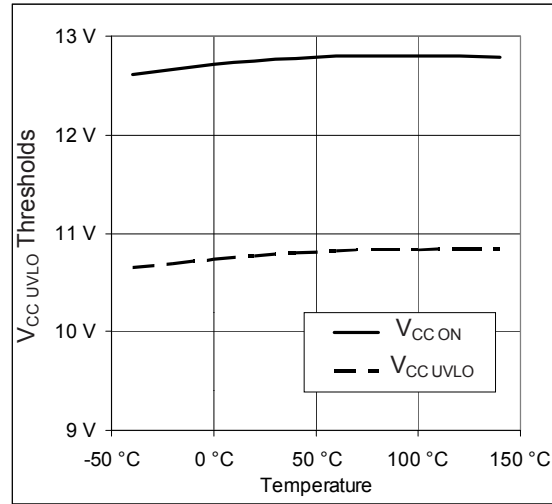


Fig. 2 - Under Voltage Lockout vs. Temperature

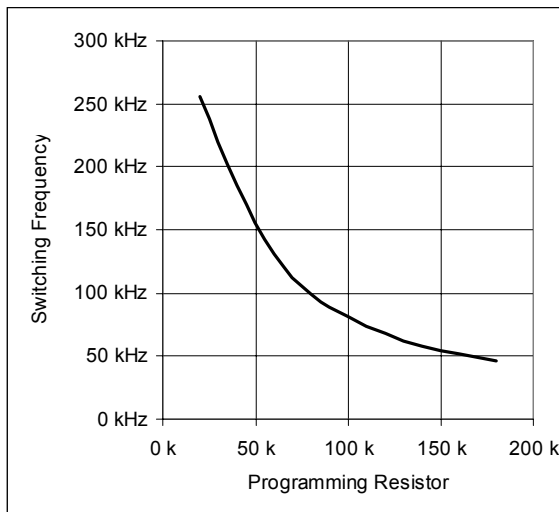


Fig. 3 - Oscillator Frequency vs. Programming Resistor

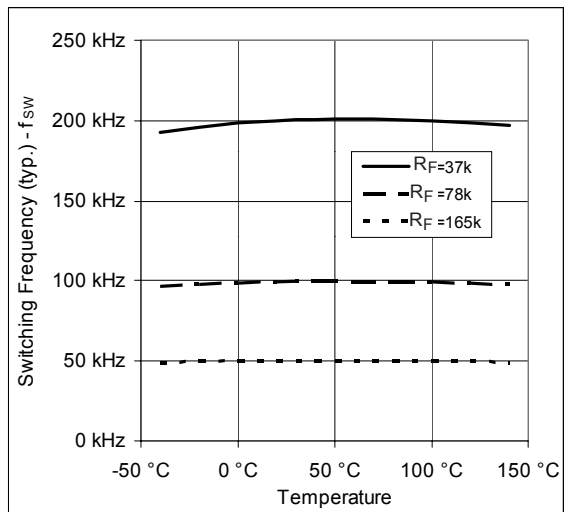


Fig. 4 - Oscillator Frequency vs. Temperature

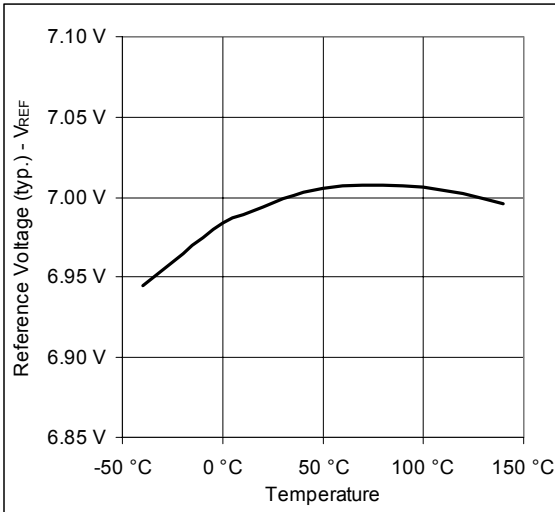


Fig. 5 - Reference Voltage

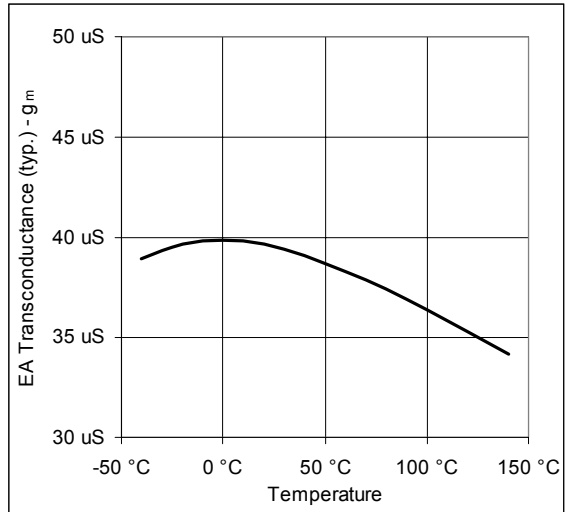


Fig. 6 - Voltage Error Amplifier Transconductance

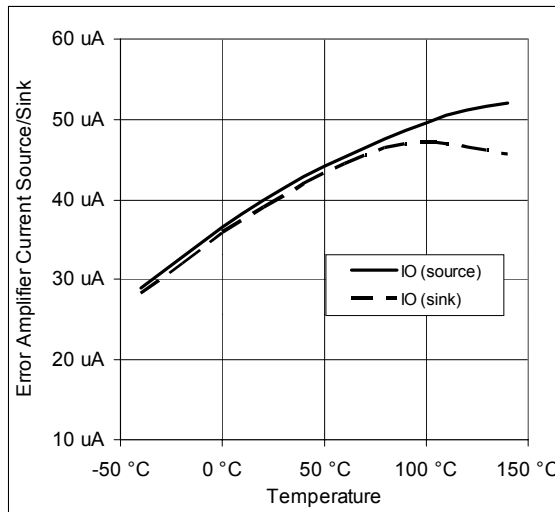


Fig.7 - Voltage Error Amplifier Source/Sink Current

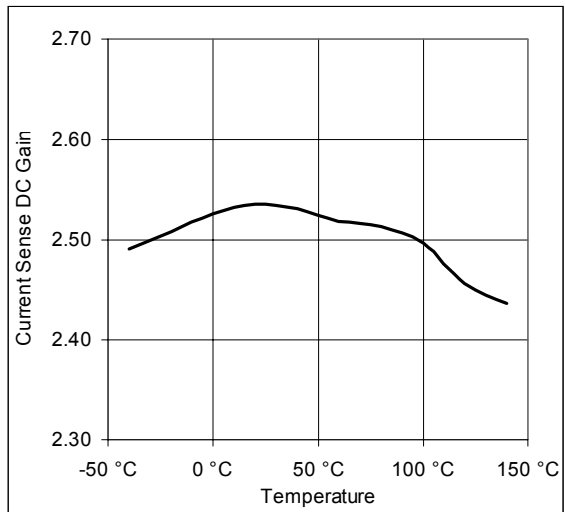
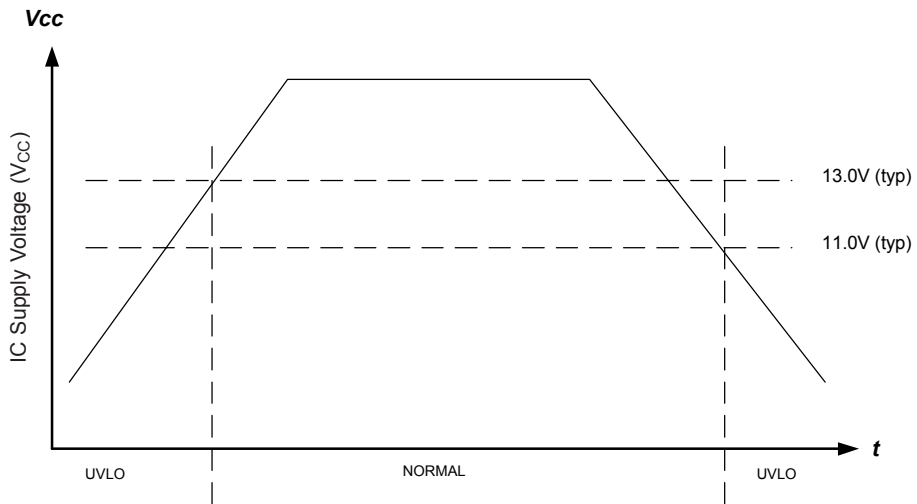
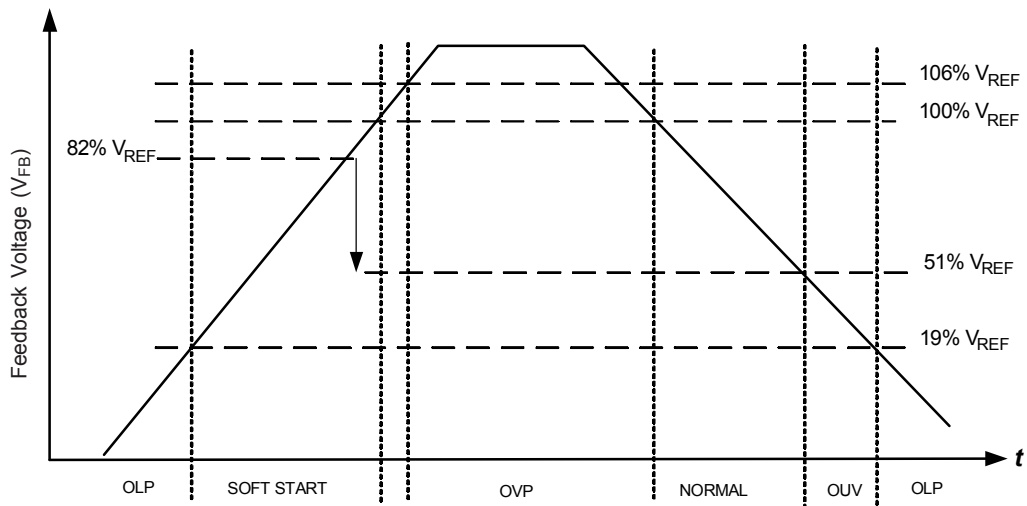


Fig. 8 - Current Sense Amplifier DC Gain

IR1150 Timing Diagrams

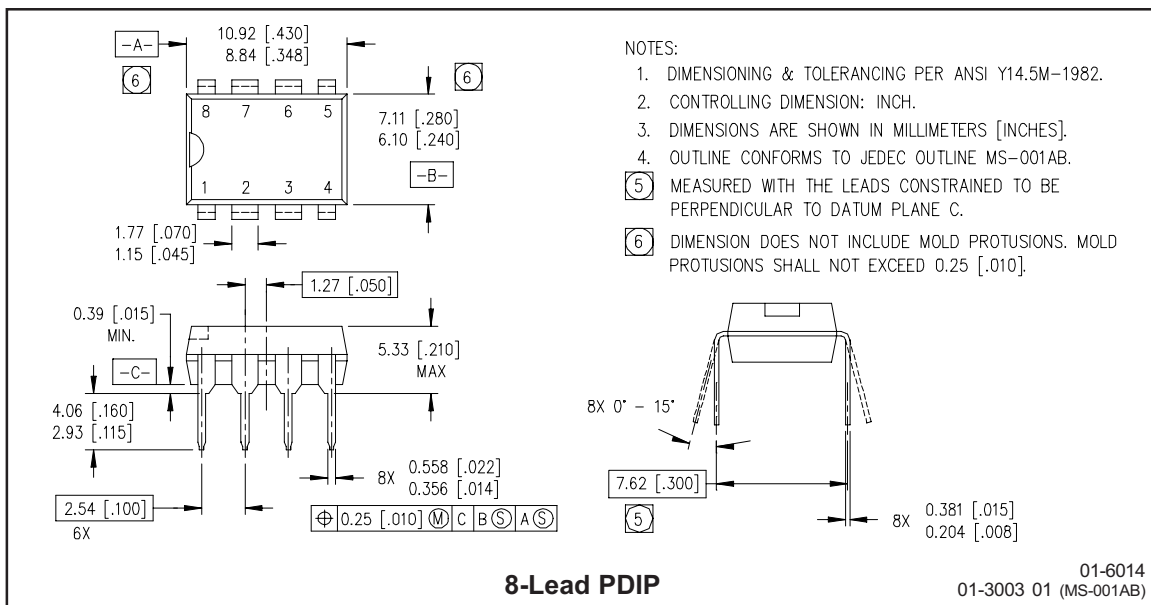
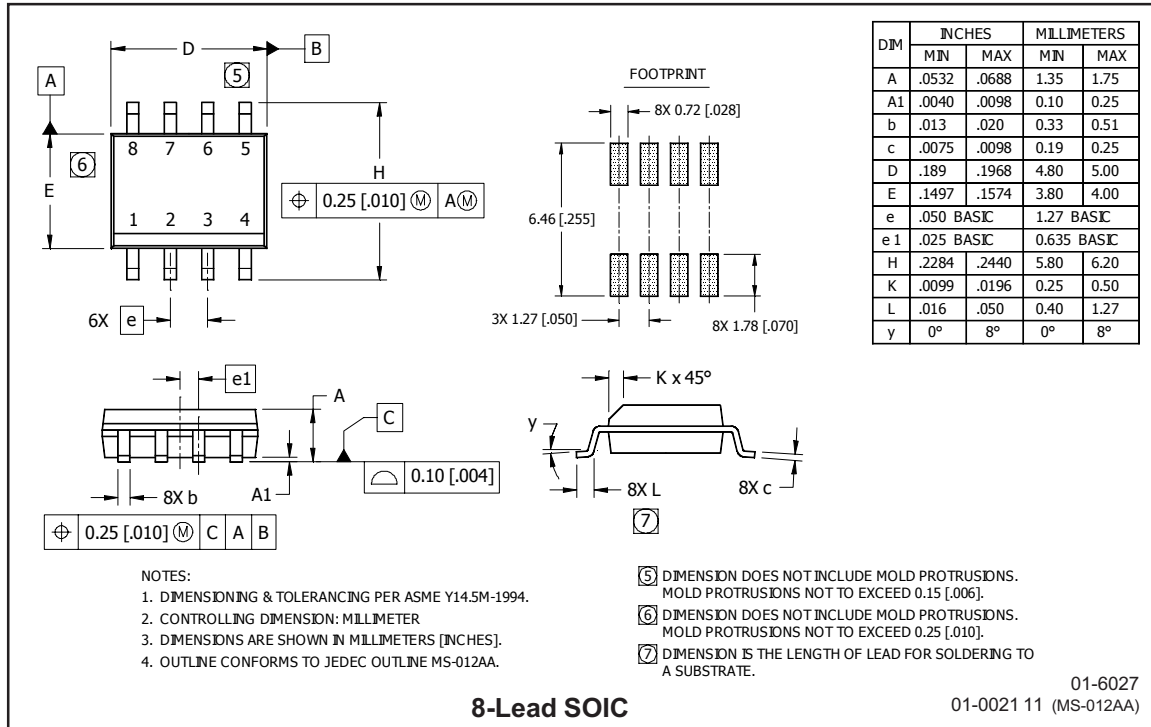


V_{CC} Under Voltage Lockout



Output Protection

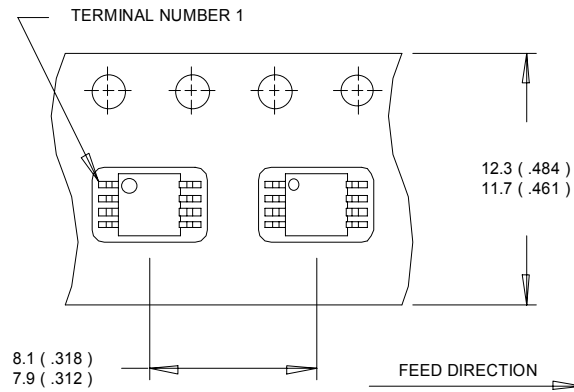
Case outline



IR1150(S)/IR1150I(S)(PbF)

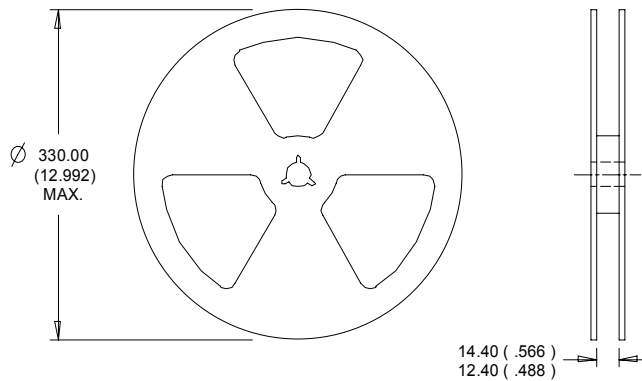
Tape & Reel Information (SOIC 8-Lead only)

Dimensions are shown in millimeters (inches)



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.

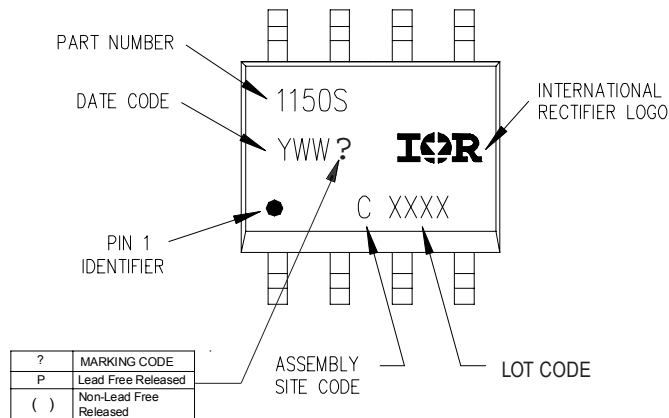


NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

PART MARKING INFORMATION

TOP MARKING (LASER)



ORDER INFORMATION

Basic Part

8-Lead SOIC IR1150STR order IR1150STR
 8-Lead SOIC IR1150ISTR order IR1150ISTR

Lead-free Part

8-Lead SOIC IR1150S order IR1150STRPbF
 8-Lead SOIC IR1150ISTR order IR1150ISTRPbF
 8-Lead PDIP IR1150 order IR1150PbF
 8-Lead PDIP IR1150I order IR1150IPbF